SY88149CL

3.3V, 1.25Gbps PECL Limiting Post Amplifier w/High Gain TTL Signal Detect

General Description

The SY88149CL is a high-sensitivity limiting post amplifier designed for use in fiber-optic receivers. These devices connect to typical transimpedance amplifiers (TIAs). The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88149CL quantizes these signals and outputs PECL level waveforms.

The SY88149CL operates from a single +3.3V power supply, over temperatures ranging from –40°C to +85°C. With its wide bandwidth and high gain, signals with data rates up to 1.25Gbps, and as small as $5mV_{pp}$, can be amplified to drive devices with PECL inputs.

The SY88149CL generates a high-gain signal-detect (SD) open-collector TTL output. The SD function has a high gain input stage for increased sensitivity. A programmable Signal Detect level set pin (SD_{LVL}) sets the sensitivity of the input amplitude detection. SD asserts high if the input amplitude rises above the threshold set by SD_{LVL} and de-asserts low otherwise. The enable input (EN) de-asserts the true output signal without removing the input signal. The SD output can be fed back to the EN input to maintain output stability under a loss-of-signal condition. Typically, 3.4dB SD hysteresis is provided to prevent chattering.

All support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- Single 3.3V power supply
- Fast SD enable/disable time
- 622Mbps to 1.25Gbps operation
- Low-noise PECL data outputs
- High-gain SD
- Chatter-free Open-Collector TTL signal detect (SD) output with internal 4.75kΩ pull-up resistor
- TTL EN input
- Programmable SD level set (SD_{LVL})
- Available in a tiny 10-pin MSOP package

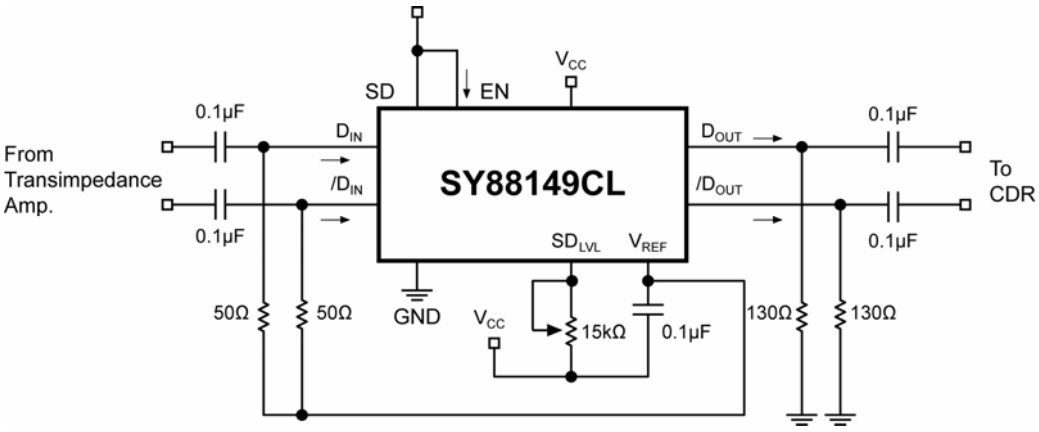
Applications

- GE-PON/GPON/EPON
- Gigabit Ethernet
- 1062Mbps Fibre Channel
- OC-12/24 SONET/SDH
- High-gain line driver and line receiver
- Low-gain TIA interface

Markets

- FTTH/FTTP
- Datacom/Telecom
- Optical transceiver

Typical Application Circuit



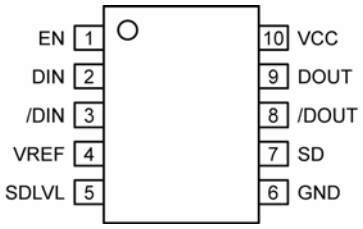
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88149CLKG	K10-1	Industrial	149C with Pb-Free bar line indicator	NiPdAu Pb-Free
SY88149CLKGTR[1]	K10-1	Industrial	149C with Pb-Free bar line indicator	NiPdAu Pb-Free

Note:

1. Tape and Reel.

Pin Configuration



10-Pin MSOP (K10-1)

Pin Description

Pin Number	Pin Name	Type	Pin Function
1	EN	TTL Input: Default is HIGH.	Enable: This input enables the outputs when it is HIGH. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open.
2	DIN	Data Input	True data input.
3	/DIN	Data Input	Complementary data input.
4	VREF		Reference voltage: Placing a capacitor here to V_{CC} helps stabilize SD_{LVL}.
5	SDLVL	Input	Signal Detect Level Set: a resistor from this pin to V_{CC} sets the threshold for the data input amplitude at which SD will be asserted.
6	GND	Ground	Device ground.
7	SD	Open-collector TTL output w/internal 4.75kΩ pull-up resistor	Signal-Detect asserts high when the data input amplitude rises above the threshold set by SD_{LVL}.
8	/DOUT	PECL Output	Complementary data output.
9	DOUT	PECL Output	True data output.
10	VCC	Power Supply	Positive power supply.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... 0V to +7.0V
Input Voltage (DIN, /DIN) ..... 0 to V_{CC}
Output Current (I_{OUT})
  Continuous ..... ±50mA
  Surge ..... ±100mA
EN Voltage ..... 0 to V_{CC}
V_{REF} Current ..... -800µA to +500µA
SD_{LVL} Voltage ..... V_{REF} to V_{CC}
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Temperature (T_J) ..... –40°C to +120°C
Junction Thermal Resistance
  MSOP (θ_{JA}) Still-air ..... 113°C/W

DC Electrical Characteristics

V_{CC} = 3.0 to 3.6V; R_L = 50Ω to V_{CC}-2V; T_A = –40°C to +85°C, typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	No output load		26	39	mA
SD_{LVL}	SD_{LVL} Voltage		V_{REF}		V_{CC}	V
V_{OH}	PECL Output HIGH Voltage		V_{CC}-1.085	V_{CC}-0.955	V_{CC}-0.880	V
V_{OL}	PECL Output LOW Voltage		V_{CC}-1.830	V_{CC}-1.705	V_{CC}-1.555	V
V_{IHCMR}	Common Mode Range		GND+2.0		V_{CC}	V
V_{REF}	Reference Voltage		V_{CC}-1.48	V_{CC}-1.32	V_{CC}-1.16	V

TTL DC Electrical Characteristics

V_{CC} = 3.0 to 3.6V; R_L = 50Ω to V_{CC}-2V; T_A = –40°C to +85°C, typical values at V_{CC} = 3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	EN Input HIGH Voltage		2.0			V
V_{IL}	EN Input LOW Voltage				0.8	V
I_{IH}	EN Input HIGH Current	V_{IN} = 2.7V V_{IN} = V_{CC}			20 100	µA µA
I_{IL}	EN Input LOW Current	V_{IN} = 0.5V	-0.3			mA
V_{OH}	SD Output HIGH Level	$V_{CC} \geq$ 3.3V, $I_{OH\text{-}MAX}$ < 160µA V_{CC} < 3.3V, $I_{OH\text{-}MAX}$ < 160µA	2.4 2.0			V V
V_{OL}	SD Output LOW Level	I_{OL} = +2mA			0.5	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Thermal performance assumes the use of a 4-layer PCB. Exposed pad must be soldered (or equivalent) to the device's most negative potential on the PCB.

AC Electrical Characteristics

V_{CC} = 3.0V to 3.6V; R_{LOAD} = 50Ω to V_{CC}–2V; T_A = –40°C to +85°C.

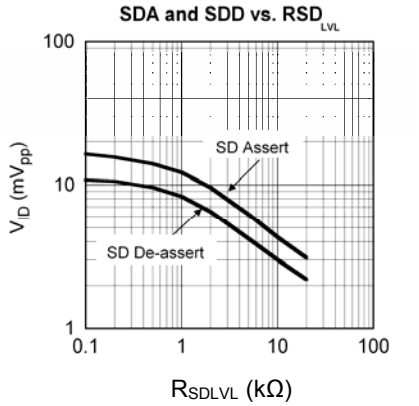
Symbol	Parameter	Condition	Min	Typ	Max	Units
t_r, t_f	Output Rise/Fall Time (20% to 80%)	Note 4			260	ps
t_{JITTER}	Deterministic Random	Note 5 Note 6		15 5		ps_{PP} ps_{RMS}
V_{ID}	Differential Input Voltage Swing	Figure 1	5		1800	mV_{PP}
V_{OD}	Differential Output Voltage Swing	$V_{ID} \geq 18mV_{PP}$ Figure 1		1500		mV_{PP}
T_{OFF}	SD Release Time			100	500	ns
T_{ON}	SD Assert Time			100	500	ns
SD_{AL}	Low SD Assert Level	R_{SDLVL} = 15kΩ, Note 8		3.4		mV_{PP}
SD_{DL}	Low SD De-assert Level	R_{SDLVL} = 15kΩ, Note 8		2.3		mV_{PP}
HYS_L	Low SD Hysteresis	R_{SDLVL} = 15kΩ, Note 7		3.4		dB
SD_{AM}	Medium SD Assert Level	R_{SDLVL} = 5kΩ, Note 8		6.2	8	mV_{PP}
SD_{DM}	Medium SD De-assert Level	R_{SDLVL} = 5kΩ, Note 8	3	4.2		mV_{PP}
HYS_M	Medium SD Hysteresis	R_{SDLVL} = 5kΩ, Note 7	2	3.4	5	dB
SD_{AH}	High SD Assert Level	R_{SDLVL} = 100Ω, Note 8		16.4	20	mV_{PP}
SD_{DH}	High SD De-assert Level	R_{SDLVL} = 100Ω, Note 8	8	10.8		mV_{PP}
HYS_H	High SD Hysteresis	R_{SDLVL} = 100Ω, Note 7	2	3.4	5	dB
B_{-3dB}	3dB Bandwidth			1		GHz
$A_{V(Diff)}$	Differential Voltage Gain			42		dB
S_{21}	Single-ended Small-Signal Gain			36		dB

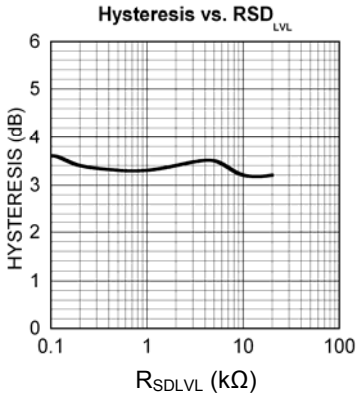
Notes:

4. Amplifier in limiting mode. Input is a 200MHz square wave.
5. Deterministic jitter measured using 1.25Gbps K28.5 pattern, V_{ID} = $10mV_{PP}$.
6. Random jitter measured using 1.25Gbps K28.7 pattern, V_{ID} = $10mV_{PP}$.
7. This specification defines electrical hysteresis as 20log(SD Assert/SD De-assert). The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2 depending upon the level of received optical power and ROSA characteristics. Based upon that ratio, the optical hysteresis corresponding to the electrical hysteresis range 2dB-5dB, shown in the AC characteristics table, will be 1dB-4dB optical Hysteresis.
8. See “Typical Operating Characteristics” for a graph showing how to choose a particular R_{SDLVL} for a particular SD assert and its associated de-assert amplitude.

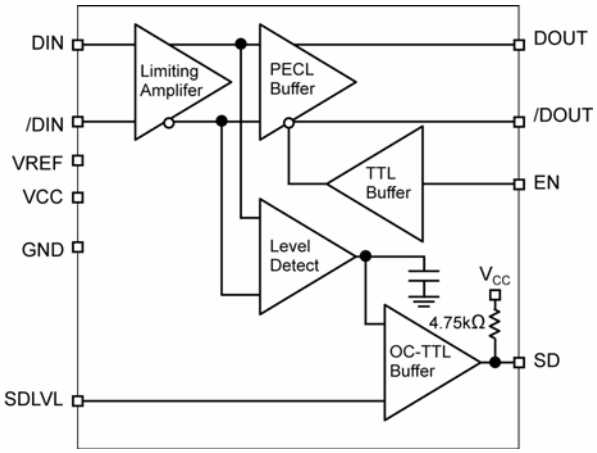
Typical Operating Characteristics

V_{CC} = 3.3V, T_A = 25°C, R_L = 50Ω to V_{CC}–2V, unless otherwise stated.





Functional Block Diagram



Detailed Description

The SY88149CL high-sensitivity limiting post amplifier operates from a single +3.3V power supply, over temperatures from –40°C to +85°C. Signals with data rates up to 1.25Gbps and as small as 5mV$_{PP}$ can be amplified. Figure 1 shows the allowed input voltage swing. The SY88149CL generates an SD output, allowing feedback to EN for output stability. SD$_{LVL}$ sets the sensitivity of the input amplitude detection.

Input Amplifier/Buffer

Figure 2 shows a simplified schematic of the input stage. The high-sensitivity of the input amplifier allows signals as small as 5mV$_{PP}$ to be detected and amplified. The input amplifier allows input signals as large as 1800mV$_{PP}$. Input signals are linearly amplified with a typically 42dB differential voltage gain. Since it is a limiting amplifier, the SY88149CL outputs typically 1500mV$_{PP}$ voltage-limited waveforms for input signals that are greater than 12mV$_{PP}$. Applications requiring the SY88149CL to operate with high-gain should have the upstream TIA placed as close as possible to the SY88149CL's input pins. This ensures the best performance of the device.

Output Buffer

The SY88149CL's PECL output buffer is designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor to V$_{CC}$–2V for each output pin provides this. Figure 3 shows a simplified schematic of the output stage.

Signal Detect

The SY88149CL generates a chatter-free Signal-Detect (SD) open-collector TTL output with internal 4.75kΩ pull-up resistor, as shown in Figure 4. SD is used to determine that the input amplitude is too small to be considered a valid input. SD asserts high if the input amplitude rises above threshold set by SDLVL and de-asserts low otherwise. SD can be fed back to the enable (EN) input to maintain output stability under a SDs of signal condition. EN de-asserts low the true output signal without removing the input signals. Typically, 3.4dB SD hysteresis is provided to prevent chattering.

Signal Detect Level Set

A programmable SD level set pin (SD$_{LVL}$) sets the threshold of the input amplitude detection. Connecting an external resistor between V$_{CC}$ and SD$_{LVL}$ sets the voltage at SD$_{LVL}$. This voltage ranges from V$_{CC}$ to V$_{REF}$. The external resistor creates a voltage divider between V$_{CC}$ and V$_{REF}$, as shown in Figure 5.

Hysteresis

The SY88149CL provides typically 3.4dB SD electrical hysteresis. By definition, a power ratio measured in dB is 10log (power ratio). Power is calculated as V^2_{IN}/R for an electrical signal. Hence the same ratio can be stated as 20log (voltage ratio). While in linear mode, the electrical voltage input changes linearly with the optical power and hence the ratios change linearly. Therefore, the optical hysteresis in dB is half the electrical hysteresis in dB given in the data sheet. The SY88149CL is an electrical device; this data sheet refers to hysteresis in electrical terms. With 3.4dB SD hysteresis, a voltage factor of 1.5 is required to assert or de-assert SD.

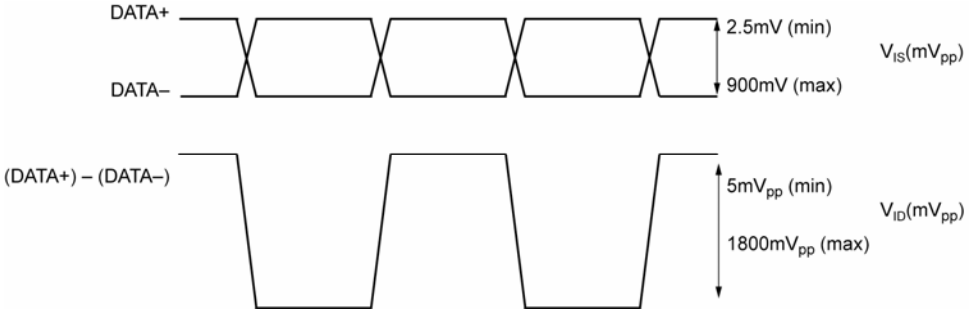


Figure 1. VIS and VID Definition

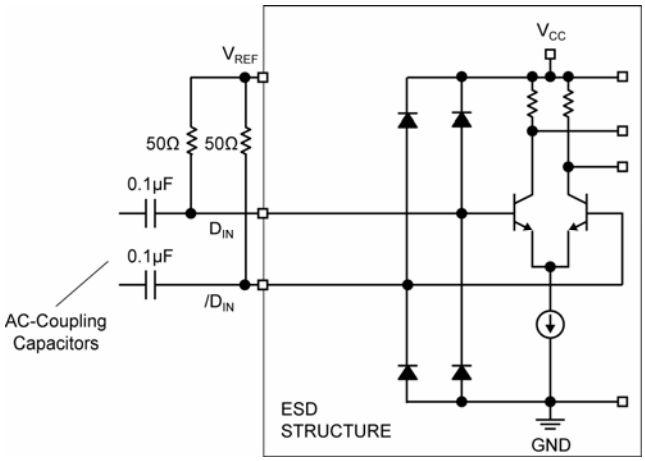


Figure 2. Input Structure

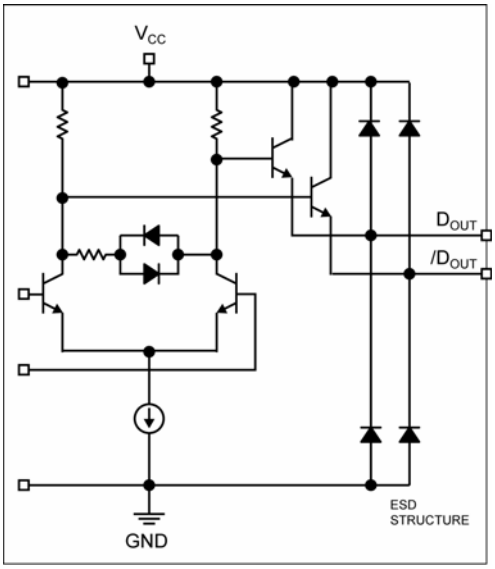


Figure 3. Output Structure

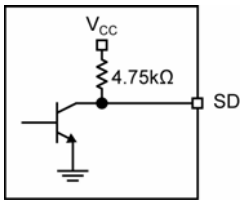


Figure 4. SD Output Structure

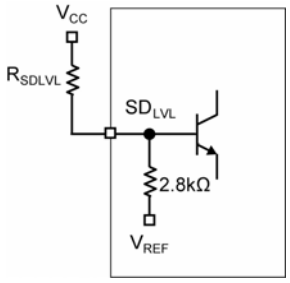


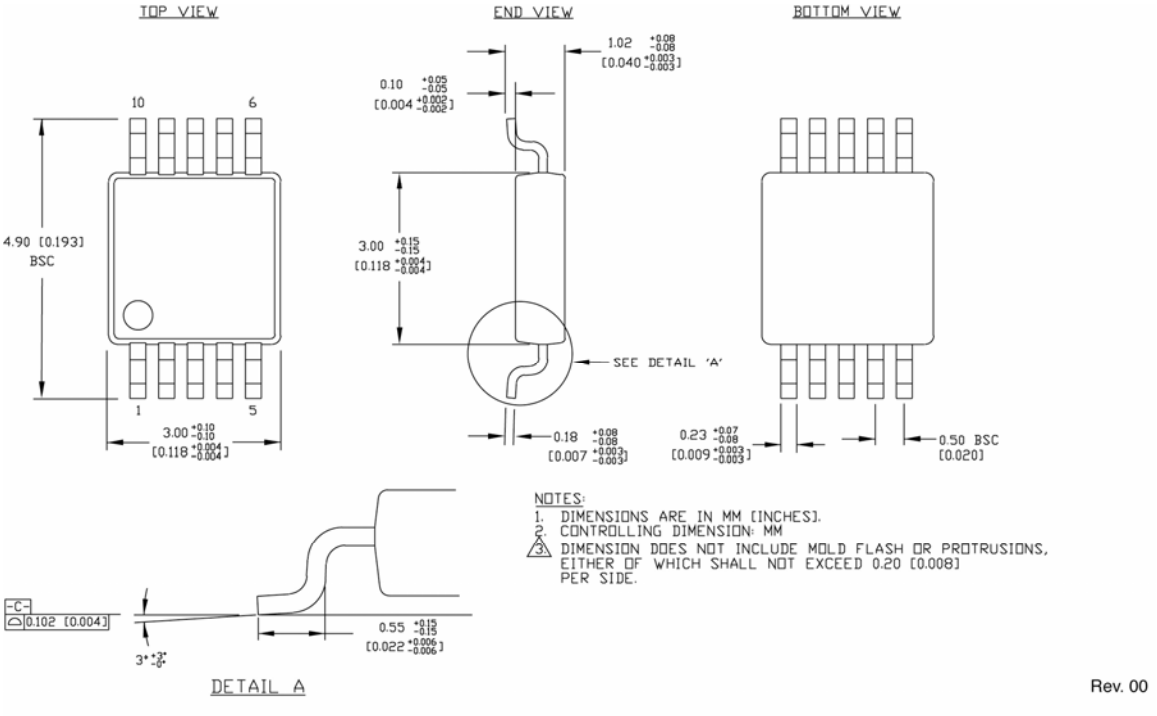
Figure 5. SD_{LVL} Setting Circuit

Note: Recommended value for R_{SDLVL} is 15kΩ or less.

Related Product and Support Documentation

Part Number	Function	Data Sheet Link
SY88933AL	3.3V/5V 1.25Gbps PECL High-Sensitivity Limiting Post Amplifier with TTL SD	http://www.micrel.com/product-info/sy88933al.shtml
Application Notes	Notes on Sensitivity and Hysteresis in Micrel Post Amplifiers	http://www.micrel.com/product-info/app_hints+notes.shtml

Package Information



10-Pin MSOP (K10-1)

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